R22 Regulation *Subject code: 4E6DC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Regular Examinations, May 2025

VLSI DESIGN

(ECE)

Maximum Marks: 60 Date: 20.06.2025 Duration: 3 hours

Note:
1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	Bloom Tx
1.a)	Define threshold voltage (Vt).	1M	1	L1
b)	Write the differences between CMOS and Bi-CMOS technologies.	1M	1	L1
c)	What is the purpose of stick diagrams in VLSI design?	1M	2	L1
d)	State any two 2μm CMOS design rules for transistors.	1M	2	L1
e)	Define fan-in and fan-out.	1M	3	L1
f)	What are the effects of wiring capacitance in VLSI circuits?	1M	3	L1
g)	List any two applications of parity generators in data path subsystems.	1M	4	L1
h)	Compare SRAM and DRAM.	1M	4	L1
i)	What is the function of a PLA in digital circuit design?	1M	5	L1
j)	Define fault coverage and its importance in CMOS testing.	1M	5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	Bloom Tx
2	a) Explain the fabrication process of n-MOS technology in detail. b) Derive the I_{DS}–V_{DS} relationship of an NMOS transistor.	5M 5M	1	L2
	OR			
3	a) Analyze the transfer characteristics of a CMOS inverter. b) Design a Bi-CMOS inverter and explain its operation.	6M 4M	1	L3
4	a) Draw stick diagrams for a 2-input NAND and NOR gate. b) Explain the layout rules for CMOS transistors.	5M 5M	1	L3
	OR			
5	a) With neat diagrams, explain the layout process of an NMOS inverter. b) Describe the impact of MOS circuit scaling.	5M 5M	2	L2
6	a) Design and analyze a 3-input CMOS NAND gate. b) Discuss the delay in driving a large capacitive load and techniques to overcome it.	5M 5M	2	L3
	OR			
7	a) Explain switch logic and compare it with static CMOS logic. b) Analyze the effect of fan-in and fan-out on delay.	5M 5M	3	L4

8	Design a 4-bit adder using VLSI design concepts.	10M	4	L3
	OR			
9	Explain the working of a comparator and a zero detector circuit.	10M	4	L2
10	a) Explain the architecture of a CPLD with a neat block diagram. b) Design a simple PLA for a given 3-variable Boolean function.	5M 5M	5	L3
	OR			
11	a) Describe the different CMOS testing techniques. b) Discuss any two design strategies for improving testability.	5M 5M	5	L3